



Tentative Product Specification

Module name: P0760WVLB-T

Issue date: 2008/06/26

Version: 1.0

Customer		
Approved by Customer		
Approved by CMEL		
PD Division	ENG Division	QA Dept

Note:

1. The information contained herein may be change without prior notice. It is therefore advisable to contact CHI MEI EL Corp. before designed your product based on this specification.
2. This tentative product specification is for reference, some item or setting maybe changed for evaluation.



Reversion History

Version	Date	Page	Description
Ver.1.0	2008/06/26	All	Tentative specification was first issued



1. Purpose:

This documentation defines general product specification for OLED module supplied by CMEL. The information described in this technical specification is tentative. Please Contact CMEL's representative while your product is modified.

2. General Description:

- Driving Mode: Active Matrix
- Color Mode: Full Color (16M color)
- Support 3-wire SPI command setting
- Interface: LVDS interface and DE only mode.
- Auto-current limit function (ACL) for power saving mode.
- Application: Portable DVD, PMP, GPS, Photo Frame etc.

3. Mechanical Data:

No.	Items	Specification	Unit
1	Diagonal Size	7.6	Inch
2	Resolution	800 RGB x 480	
3	Pixel Pitch	207 x 207	um
4	Active Area	165.60 x 99.36	mm
5	Outline Area	177.30 x 118.32	mm
6	Thickness	Max 5.3	mm
7	Weight	TBD	g

4. Maximum ratings:

Symbol	Parameter	Value	Unit	Note
VCI	Supply Voltage	TBD	V	(1)
TA	Operating Temperature	TBD	°C	(1)
Tstg	Storage Temperature	TBD	°C	(1)

Note (1) Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section. Unused outputs must be left open.

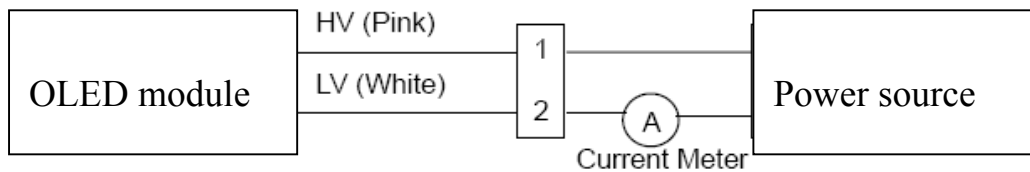
5. Electrical Characteristic:

5.1 DC Characteristic—module

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VCI	4.5	5	5.5	V	-
Permissive Ripple Voltage	V _{PR}		TBD		mV	
Rush Current	I _{RUSH}		TBD		A	(2)
Initial Stage Current	I _{IS}		TBD		A	(2)

5.2 DC Characteristic—OLED

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Positive power	VDD		TBD		V	-
Negative power	VSS		RBD		V	
Lamp Current	I _L		TBD		A	



Note (2) TBD.



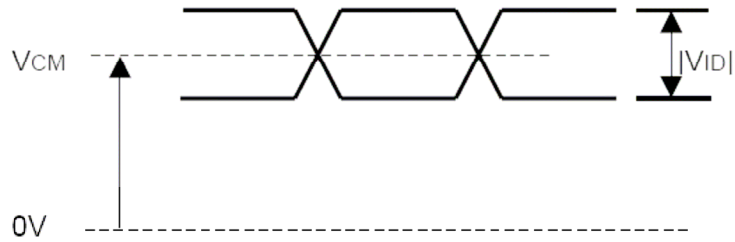
5.3 AC Characteristic—LVDS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$			+100	mV	(3)
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100			mV	(3)
LVDS Common Mode Voltage	V_{CM}	1.125	1.2	1.375	V	(3)
OLED Diode Refer Voltage	$ V_{ID} $	100		600	mV	(3)
Terminating Resistor	R_T		100		Ohm	
DCLK frequency	F_{CPH}	23.51	24.70	-	MHz	(4)
DCLK period	T_{CPH}	-	40.48	42.53	ns	(4)
DCLK pulse duty	T_{CWH}	-	50	-	%	(4)
DE pulse width	T_{EP}	-	800	-	T_{CPH}	(4)
HSYNC pulse width	T_{WH}	1	3	-	T_{CPH}	(4)
HSYNC-first horizontal data time	T_{HBP}	3	20	-	T_{CPH}	(4)
HSYNC front porch	T_{HFP}	0	10	-	T_{CPH}	(4)
HSYNC period	T_H	803	830	-	T_{CPH}	(4)
VSYNC pulse width	T_{WV}	1	3	-	T_H	(4)
VSYNC-1 st Data input (DE) time	T_{VBP}	3	10	-	T_H	(4)
VSYNC front porch	T_{VFP}	5	6	-	T_H	(4)
VSYNC period	T_V	488	496	-	T_H	(4)

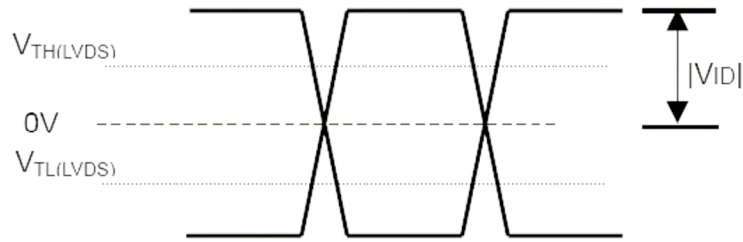
Note (3) The parameters of LVDS signals are defined as the following figures.



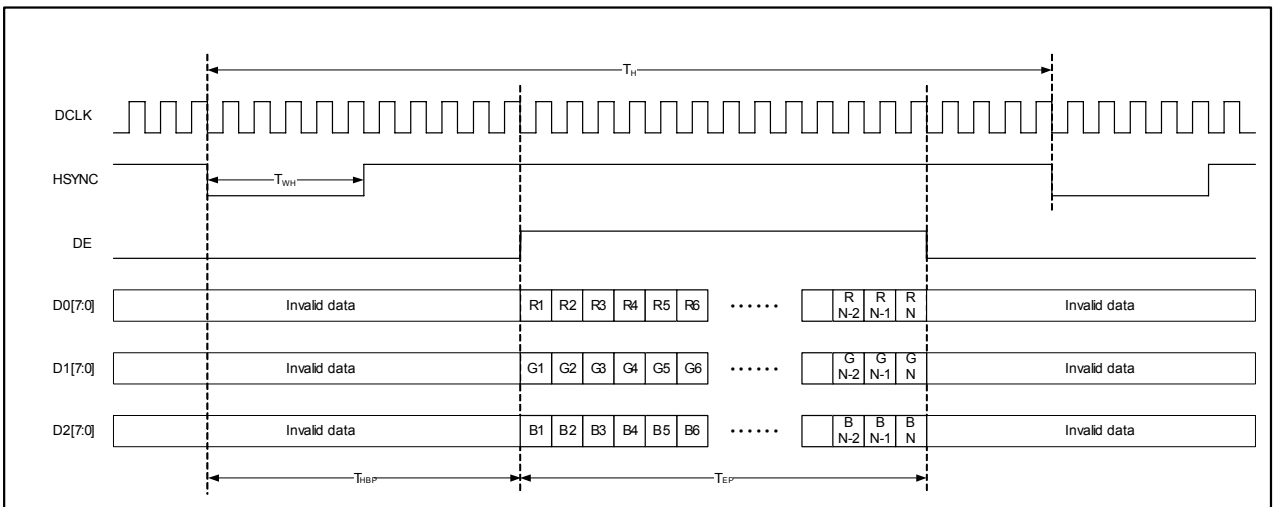
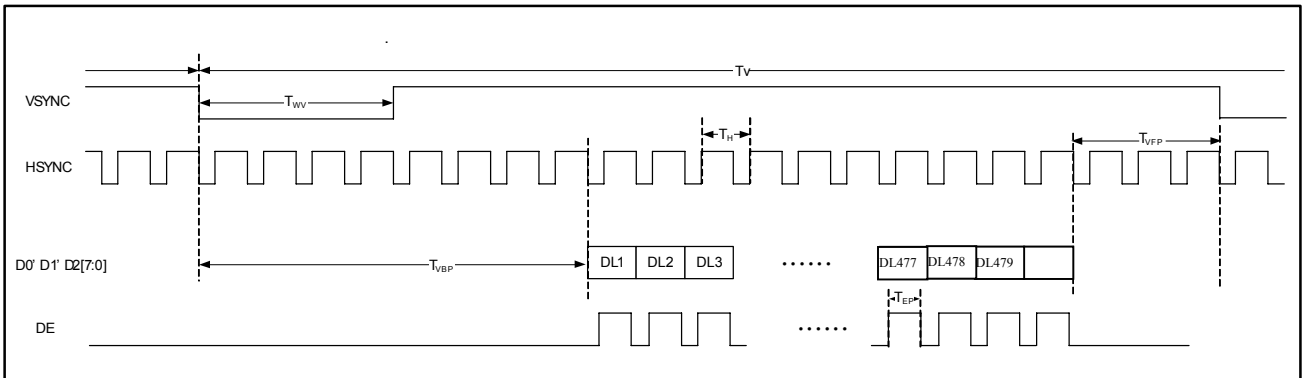
Single Ended



Differential



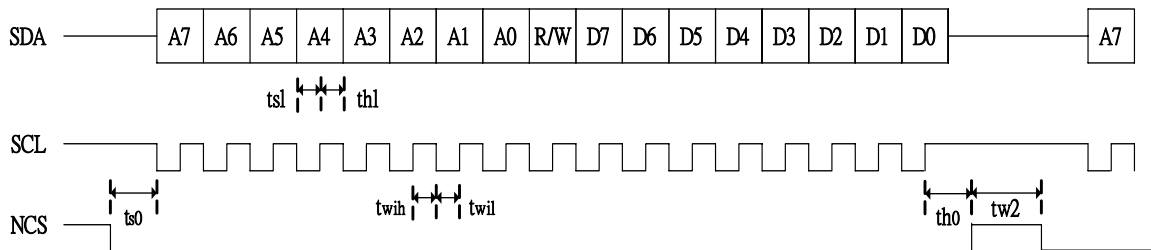
Note (4) The timing specification of LVDS signals are defined as the following figures.





5.4 AC Characteristic—SPI

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Time from NCS to SCL	Ts0	40			ns	
Time from SCL to NCS	Th0	60			ns	
SCL low time	Twih		Tcyc/2		ns	
SCL high time	Twil		Tcyc/2		ns	
Setup time of SDA	Tsl	40			ns	
Hold time of SDA	Thl	40			ns	
NCS high pulse width	Tw2	500			ns	
Serial clock cycle time	Tcyc	100	500		ns	
Time from NCS to SCL	Ts0	40			ns	
Time from SCL to NCS	Th0	60			ns	
SCL low time	Twih		Tcyc/2		ns	





6. Electro-Optical Characteristic:

Items	Symbol	Min	Typ.	Max	Unit	Remark
Luminance	L	170	200	230	Cd/m ²	(1)(5)
Power Consumption	Pon			TBD	W	30% pixels on (1)
Response Time	Tres			50	uS	(2)
Color Gamma	NTSC		70		%	(1)
CIE _x (White)	W _x		0.31		-	(5)
CIE _y (White)	W _y		0.33		-	(5)
Viewing Angle	VA	160			Degree	(3)
Contrast	CR	10000:1				(4)
Operation Lifetime	LTop	20000			Hrs	(1)(6)

Note:

Measuring surrounding: dark room

Surrounding temperature: 25°C

1. Test condition:

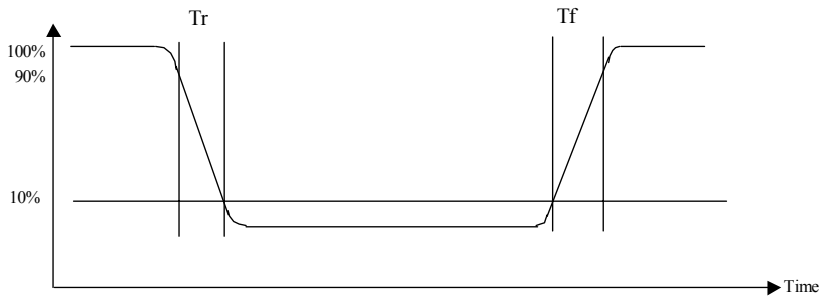
We turn on 4% area in the center of panel, and fix full white 200nits to adjust gamma code.

- a. AR_VDD=TBD, AR_VSS= TBD
- b. IC Initial Register Setting: TBD

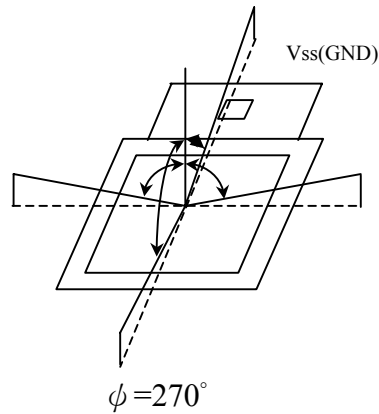




2. Response Time test condition



3. Viewing angle test condition:



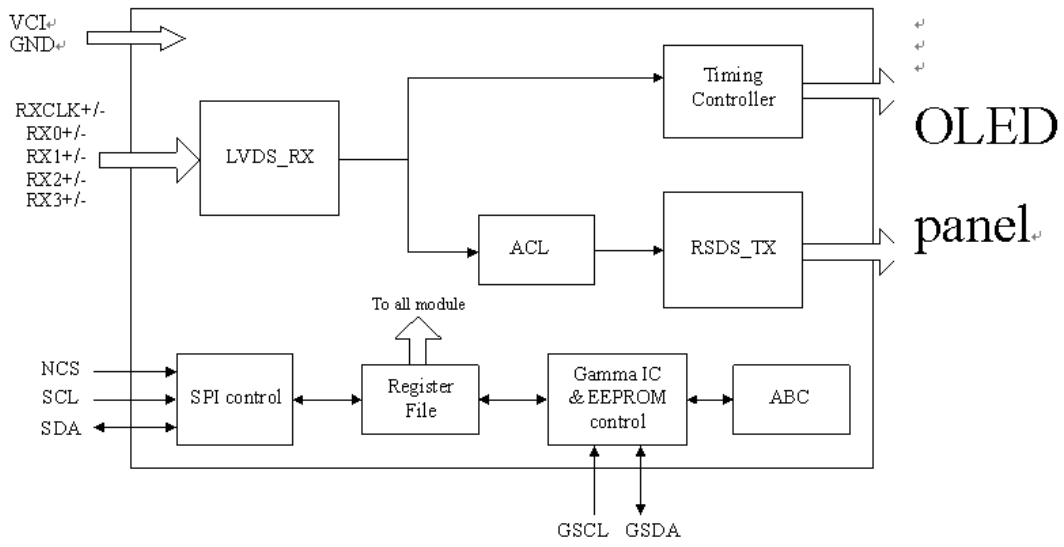
4. Contrast

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

5. Optical tester: CA210

6. Operation Life Time is defined when the luminance decay to less than 50% of the initial luminance during the average operation. The Luminance of the average operation is defined 30% maximum luminance.

7. System Diagram:



8. Input Terminal Pin Assignment:

8.1 OLED module

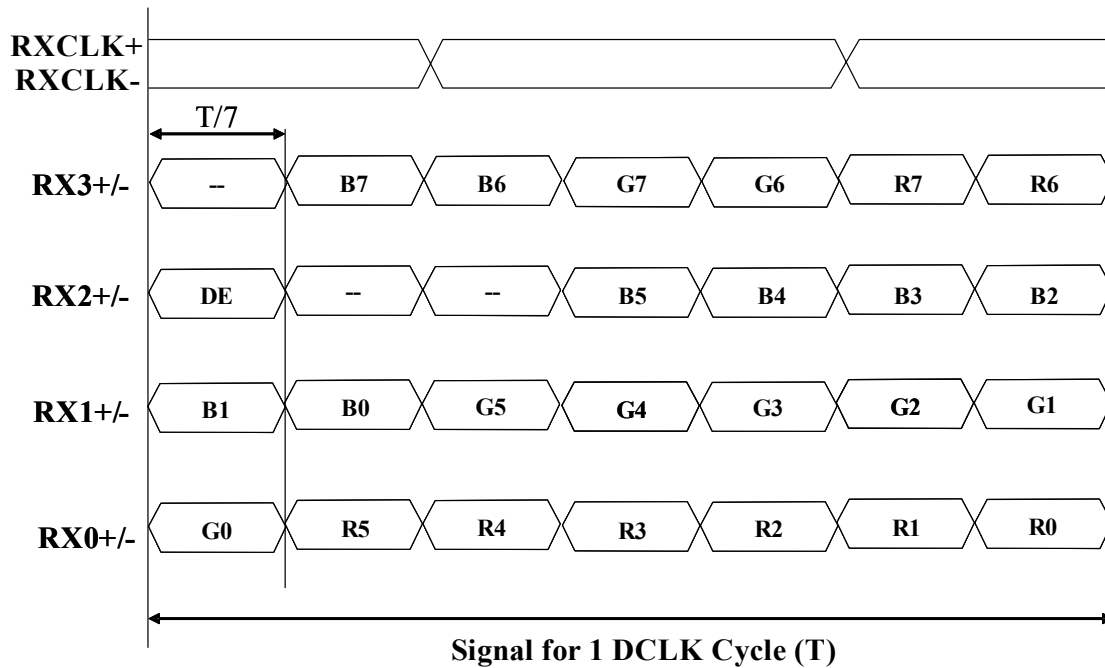
PIN	Symbol	I/O	Description	Remarks
1	VCI	P	Power supply 5V (typical)	5V
2	GND	P	Ground	Ground
3	NC	-	Not connect	Open
4	NC	-	Not connect	Open
5	NC	-	Not connect	Open
6	NC	-	Not connect	Open
7	NC	-	Not connect	Open
8	RX0-	I	Negative LVDS differential data input, Channel 0	RX0-
9	RX0+	I	Positive LVDS differential data input, Channel 0	RX0+
10	GND	P	Ground	Ground
11	RX1-	I	Negative LVDS differential data input, Channel 1	RX1-
12	RX1+	I	Positive LVDS differential data input, Channel 1	RX1+
13	GND	P	Ground	Ground
14	RX2-	I	Negative LVDS differential data input, Channel 2	RX2-
15	RX2+	I	Positive LVDS differential data input, Channel 2	RX2+
16	GND	P	Ground	Ground
17	RXCLK-	I	Negative LVDS differential clock input	RXCLK-
18	RXCLK+	I	Positive LVDS differential clock input	RXCLK+
19	GND	P	Ground	Ground
20	RX3-	I	Negative LVDS differential data input, Channel 3	RX3-
21	RX3+	I	Positive LVDS differential data input, Channel 3	RX3+
22	GND	P	Ground	Ground
23	GND	P	Ground	Ground
24	GND	P	Ground	Ground
25	GND	P	Ground	Ground
26	SCL	I	Serial interface clock pin.	SCL
27	SDA	I/O	Serial interface data input and output line	SDA
28	NCS	I	Serial interface chip enable line	NCS
29	VCI	P	Power supply 5V (typical)	5V
30	VCI	P	Power supply 5V (typical)	5V



8.2 OLED unit

PIN	Symbol	I/O	Description	Remarks
1	VDD	P	Positive power	Pink
2	VSS	P	Negative power	White

8.3 Timing Diagram of LVDS input signal



8.4 Register description:

NAME	ADDR	R/W	Description
TCONCTL6	06h	R/W	[7:0] VFP: 0x00: 5HSYNC (default) 0x01: 6HSYNC 0xFE: 259 HSYNC 0xFF: 260 HSYNC Default: 00h
TCONCTL7	07h	R/W	[7:0] HBP: Horizontal valid data start time select.



			<p>0x00 : 3 DCLK 0x01 : 4 DCLK 0x11 : 20 DCLK (default) 0xFE : 257 DCLK 0xFF : 258 DCLK</p> <p>Default: 11h</p>
TCONCTL8	08h	R/W	<p>[7:0] HFP: 0x00: 0 DCLK 0x01: 1 DCLK 0x0A: 10 DCLK (default) 0xFE: 254 DCLK 0xFF: 255 DCLK</p> <p>Default: 0Ah</p>
SERCTL1	57h	R/W	<p>[6:0] CNTR: GSCL frequency setting parameter GSCL frequency = DCLK / ((CNTR+1) x2) Ex. 24.7Mhz/((31+1) x2) = 24.7Mhz/64 = 386Khz</p> <p>Default: 1Fh</p>
GAMCTL2	59h	R/W	<p>[7] BKSEL: select gamma ic memory bank 0: select bank 0 1: select bank 1 [6] A0 0: select gamma ic 1 1: select gamma ic 2 [5:0] STRADR: gamma output voltage selected address, when BUR_WRT (5Bh bit 4) is 1, STRADR represents gamma output voltage start address, other mode represent the selected address of gamma ic</p> <p>Default: 00h</p>
GAMCTL3	5Ah	R/W	<p>[7] GI2CBUSY (read only): any action of gamma ic and EEPROM must check this bit</p>



			<p>0: I2C bus not busy 1: I2C bus busy</p> <p>[5:0] ENDADR: this is useful only at BUR_WRT (5Bh bit 4) is 1, and represents the gamma output voltage end address</p> <p>Default: 17h</p>
GAMCTL4	5Bh	WC	<p>[6] GEN_RST: reset gamma ic [5] SIN_WRT: single write gamma DAC register [4] BUR_WRT: burst write gamma DAC register [3] WRT_MEM: single write gamma ic OTP [2] SIN_READ: single read gamma DAC register [1] GEN_ACQ: general acquire gamma ic OTP to gamma DAC output [0] SIN_ACQ: single acquire gamma ic OTP to gamma DAC output</p> <p>Default: 00h</p>
GAMCTL5	5Ch	R	[1:0] RDDATA [9:8]: high byte of read DAC register from gamma ic
GAMCTL 6	5Dh	R	[7:0] RDDATA [7:0]: low byte of read DAC register from gamma ic
EEPROM1	5Eh	R/W	<p>[6:4] BANKSEL: select EEPROM read/write bank 000: write 5Fh ~ 86h to EEPROM bank 0 or read EEPROM bank 0 to 5Fh ~ 86h 001: write 5Fh ~ 86h to EEPROM bank 1 or read EEPROM bank 1 to 5Fh ~ 86h 010: write 5Fh ~ 86h to EEPROM bank 2 or read EEPROM bank 2 to 5Fh ~ 86h 011: write 5Fh ~ 86h to EEPROM bank 3 or read EEPROM bank 3 to 5Fh ~ 86h 1xx: write 00h ~ 5Eh to EEPROM bank4 or read EEPROM bank4 to 00h ~ 5Eh</p> <p>[1] EEPROM_WR (write & clear): EEPROM write [0] EEPROM_RD (write & clear): EEPROM read</p> <p>Default: 40h</p>



RGAMMA01	5Fh	R/W	[7:6] DAC4 [9:8]: R_GAMMA30 high byte [5:4] DAC3 [9:8]: R_GAMMA15 high byte [3:2] DAC2 [9:8]: R_GAMMA5 high byte [1:0] DAC1 [9:8]: R_GAMMA0 high byte Default:
RGAMMA02	60h	R/W	[7:0] DAC1 [7:0]: R_GAMMA0 low byte Default:
RGAMMA03	61h	R/W	[7:0] DAC2 [7:0]: R_GAMMA5 low byte Default:
RGAMMA04	62h	R/W	[7:0] DAC3 [7:0]: R_GAMMA15 low byte Default:
RGAMMA05	63h	R/W	[7:0] DAC4 [7:0]: R_GAMMA30 low byte Default:
RGAMMA06	64h	R/W	[7:6] DAC8 [9:8]: R_GAMMA255 high byte [5:4] DAC7 [9:8]: R_GAMMA168 high byte [3:2] DAC6 [9:8]: R_GAMMA84 high byte [1:0] DAC5 [9:8]: R_GAMMA50 high byte Default:
RGAMMA07	65h	R/W	[7:0] DAC5 [7:0]: R_GAMMA50 low byte Default:
RGAMMA08	66h	R/W	[7:0] DAC6 [7:0]: R_GAMMA84 low byte Default:
RGAMMA09	67h	R/W	[7:0] DAC7 [7:0]: R_GAMMA168 low byte Default:
RGAMMA10	68h	R/W	[7:0] DAC8 [7:0]: R_GAMMA255 low byte Default:
GGAMMA01	69h	R/W	[7:6] DAC12 [9:8]: G_GAMMA30 high byte [5:4] DAC11 [9:8]: G_GAMMA15 high byte



			[3:2] DAC10 [9:8]: G_GAMMA5 high byte [1:0] DAC9 [9:8]: G_GAMMA0 high byte Default:
GGAMMA02	6Ah	R/W	[7:0] DAC9 [7:0]: G_GAMMA0 low byte Default:
GGAMMA03	6Bh	R/W	[7:0] DAC10 [7:0]: G_GAMMA5 low byte Default:
GGAMMA04	6Ch	R/W	[7:0] DAC11 [7:0]: G_GAMMA15 low byte Default:
GGAMMA05	6Dh	R/W	[7:0] DAC12 [7:0]: G_GAMMA30 low byte Default:
GGAMMA06	6Eh	R/W	[7:6] DAC16 [9:8]: G_GAMMA255 high byte [5:4] DAC15 [9:8]: G_GAMMA168 high byte [3:2] DAC14 [9:8]: G_GAMMA84 high byte [1:0] DAC13 [9:8]: G_GAMMA50 high byte Default:
GGAMMA07	6Fh	R/W	[7:0] DAC13 [7:0]: G_GAMMA50 low byte Default:
GGAMMA08	70h	R/W	[7:0] DAC14 [7:0]: G_GAMMA84 low byte Default:
GGAMMA09	71h	R/W	[7:0] DAC15 [7:0]: G_GAMMA168 low byte Default:
GGAMMA10	72h	R/W	[7:0] DAC16 [7:0]: G_GAMMA255 low byte Default:
BGAMMA01	73h	R/W	[7:6] DAC20 [9:8]: B_GAMMA30 high byte [5:4] DAC19 [9:8]: B_GAMMA15 high byte [3:2] DAC18 [9:8]: B_GAMMA5 high byte [1:0] DAC17 [9:8]: B_GAMMA0 high byte



			Default:
BGAMMA02	74h	R/W	[7:0] DAC17 [7:0]: B_GAMMA0 low byte Default:
BGAMMA03	75h	R/W	[7:0] DAC18 [7:0]: B_GAMMA5 low byte Default:
BGAMMA04	76h	R/W	[7:0] DAC19 [7:0]: B_GAMMA15 low byte Default:
BGAMMA05	77h	R/W	[7:0] DAC20 [7:0]: B_GAMMA30 low byte Default:
BGAMMA06	78h	R/W	[7:6] VCOM2 [9:8]: B_GAMMA255 high byte [5:4] VCOM1 [9:8]: B_GAMMA168 high byte [3:2] DAC22 [9:8]: B_GAMMA84 high byte [1:0] DAC21 [9:8]: B_GAMMA50 high byte Default :
BGAMMA07	79h	R/W	[7:0] DAC21 [7:0]: B_GAMMA50 low byte Default:
BGAMMA08	7Ah	R/W	[7:0] DAC22 [7:0]: B_GAMMA84 low byte Default:
BGAMMA09	7Bh	R/W	[7:0] VCOM1 [7:0]: B_GAMMA168 low byte Default:
BGAMMA10	7Ch	R/W	[7:0] VCOM2 [7:0]: B_GAMMA255 low byte Default:
WGAMMA01	7Dh	R/W	[7:6] DAC34 [9:8]: W_GAMMA30 high byte [5:4] DAC33 [9:8]: W_GAMMA15 high byte [3:2] DAC32 [9:8]: W_GAMMA5 high byte [1:0] DAC31 [9:8]: W_GAMMA0 high byte Default:

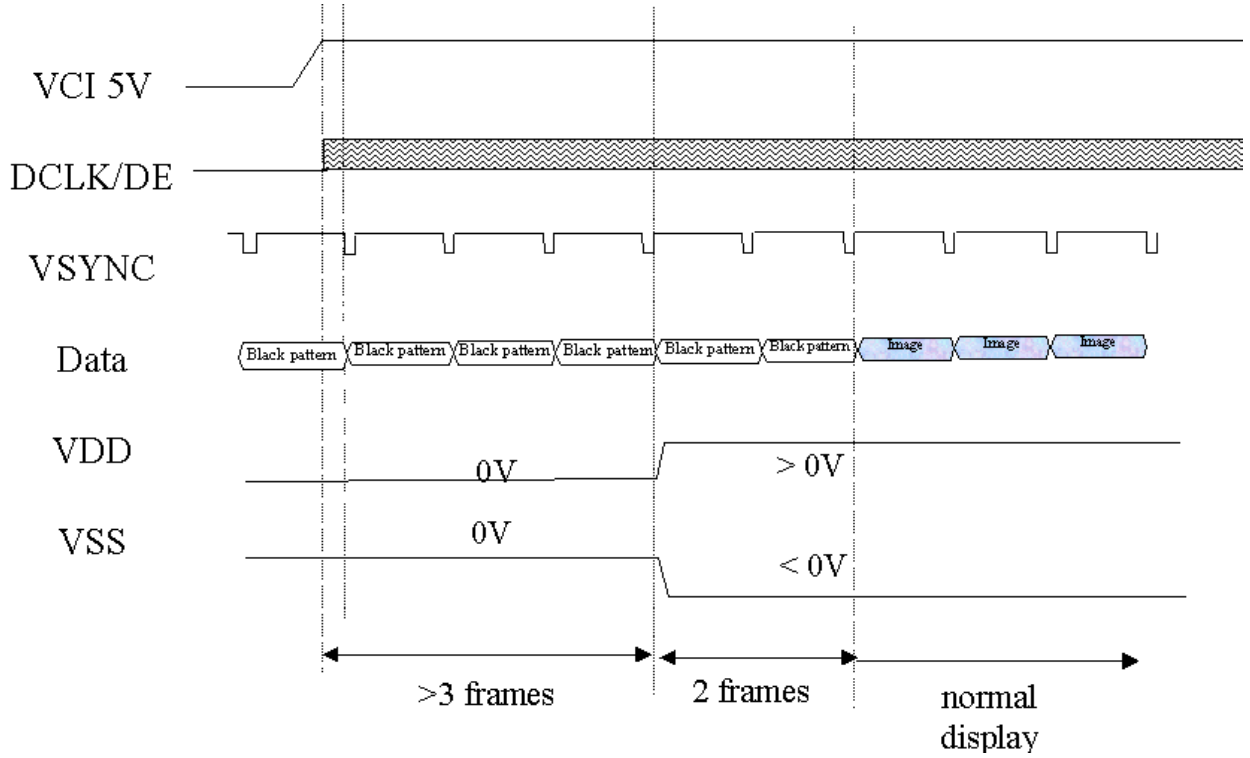


WGAMMA02	7Eh	R/W	[7:0] DAC31 [7:0]: W_GAMMA0 low byte Default:
WGAMMA03	7Fh	R/W	[7:0] DAC32 [7:0]: W_GAMMA5 low byte Default:
WGAMMA04	80h	R/W	[7:0] DAC33 [7:0]: W_GAMMA15 low byte Default:
WGAMMA05	81h	R/W	[7:0] DAC34 [7:0]: W_GAMMA30 low byte Default:
WGAMMA06	82h	R/W	[7:6] DAC38 [9:8]: W_GAMMA255 high byte [5:4] DAC37 [9:8]: W_GAMMA168 high byte [3:2] DAC36 [9:8]: W_GAMMA84 high byte [1:0] DAC35 [9:8]: W_GAMMA50 high byte Default:
WGAMMA07	83h	R/W	[7:0] DAC35 [7:0]: W_GAMMA50 low byte Default:
WGAMMA08	84h	R/W	[7:0] DAC36 [7:0]: W_GAMMA84 low byte Default:
WGAMMA09	85h	R/W	[7:0] DAC37 [7:0]: W_GAMMA168 low byte Default:
WGAMMA10	86h	R/W	[7:0] DAC38 [7:0]: W_GAMMA255 low byte Default:
EEPROM2	FFh	R/W	[0] EE_RDEN: this bit have to use with EEPROM_WR (5Eh bit1), when this bit set high first and write EEPROM_WR = 1, the register 00h ~ 5Eh default value are download by EEPROM after the system power on Default:

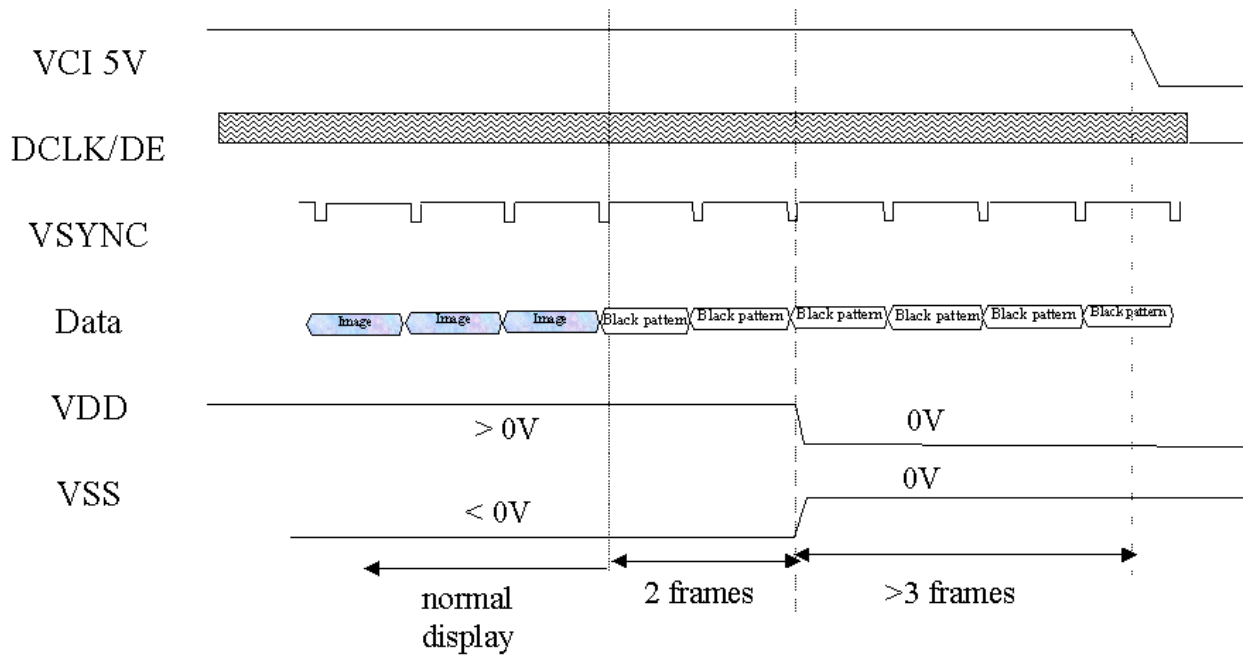


9. Power sequence.

9.1 Power on sequence

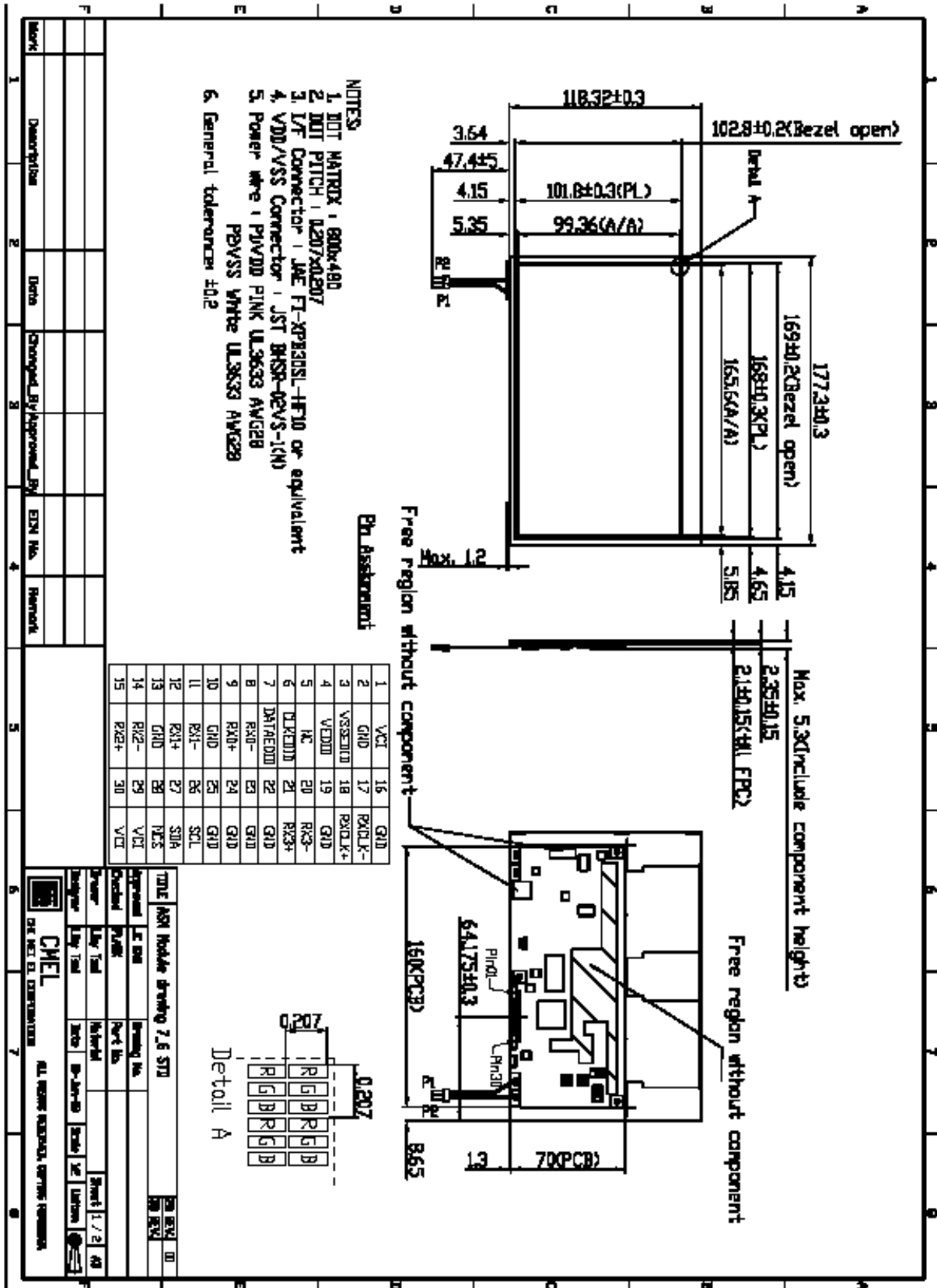


9.2 Power off sequence





10. External Dimension:





11. Reliability Test:

TBD



12. Package:

TBD